

Amendment to the Specification

Please replace the paragraph [0038] with the following:

[0038] The prior art processor cited above has a 32-bit architecture. It is, however desirable that a 64 bit architecture still supports former 32 bit instructions originating from the use of earlier developed programs. Thus, predetermined protocol convention exist in prior art that in case of writing a 32-bit result into a 64-bit register the "overhanging" bits have to remain unchanged. For most of the instructions this creates no particular problem, since for most instructions one of the source registers 410, 415 is the same as the target register 420. Hence, the unchanged 32-bits of the result 0 . . . 31 is available as input to the execution unit and it can be used to set the 32 bit part of the 64 bit result that does not have to be calculated.

Please replace the paragraph [0040] with the following:

[0040] In an out-of-order processor, however, the IWB can contain many instructions at a time with their speculative results being calculated. Since the LA instruction may be followed by a 64 bit instruction that has as a source R1 dependent on the LA instruction result, all 64 bits need to be available in the Reservation station.